**AIM:**

To write Verilog code for

1. 4 bit Wallace tree Multiplier

And find Timing, Area, Power , Delay and RTL Schematics in Xilinx and Cadence.

**INTRODUCTION:**

Xilinx and Cadence are software used to analyse the combinational circuits we make. We have used Xilinx, Cadence to find Area, Timing, Power , Delay, RTL Schematics. Basically bigger the circuit, more the transistors, more the area, more the power. These software help in getting a better understanding of combinational circuits at transistor level, ASIC and FPGA.

**PROCEDURE:**

Write Verilog codes in Xilinx with the test benches.

See their RTL schematics, Area, Power, Delay, timing diagrams in Xilinx, nclaunch.

Make area and power diagrams using genus and innovus.

Make separate files and compare.

**RESULTS:**

Area in um^2 in Genus and Innovus , Power in nW

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Q | Area | Area | Area | Power | Power | Power |
| Tool | Xilinx | Genus | Innovus | Xilinx | Genus | Innovus |
| 1 | - | 303.517 | 303.5169 | 0.081 W | 11141.001 | 7962 |

AREA OF XILINX:

Selected Device : 3s500efg320-5

Number of Slices: 19 out of 4656 0%

Number of 4 input LUTs: 33 out of 9312 0%

Number of IOs: 16

Number of bonded IOBs: 16 out of 232 6%

**Delay = 12.162 ns**

**CONCLUSION:**

We wrote Verilog codes and compared area and power for each question.

As circuit size increases, area increases, power increases.

Also Innovus is more accurate than genus.

Innovus optimizes the circuit and gives less power.

**REFERENCES:**

www.asic-world.com